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Bidirectional On-Board Charger Based on Vienna Rectifier Topology

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Abstract— **This paper addresses the problem of the negative impact of the electrical vehicles on the grid and the low efficiency and power density drawbacks of the EV chargers. The solution is to choose the efficient topology of the Front-end rectifier in order to solve both the pollution of the grid by power factor correction, and the low efficiency of EV Charger by reducing the stress of the component which will reduce the cooling system needed and consequently increase power density of the system. This topology can be used in V2X charger. Modeling and control design of the front-end rectifier is investigated in the d-q reference.**

Keywords— OBC; electrical vehicle; efficiency; V2X charger; Battery; converter topology.

I. INTRODUCTION

In the past decade, there is growing awareness about line pollution and deteriorating power factor due to all pervading inductive and non-linear loads. Electrical vehicles and aircraft are an important part of the no-linear loads that affect the electrical infrastructure [1,2,4].

This evolution toward more EVs has a lot of challenges especially in the On-Board Charger OBC, due to the limitation of the interior space, onboard charger (OBC) needs to meet the requirements of high power-density ($\frac{kW}{dm^3}$), high charging efficiency, good heat dissipation effect, and unity power factor which decrease the stress on conventional grid, thus decrease the cost of charging [5].

Before introducing the solution to improve the quality of EV charging system, let have a look on the architecture of the On-Board Chargers fig.1 [7, 9].
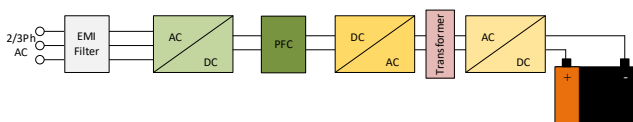

Fig.1 OBC's bloc diagram.

Charging at home is the most preferable way for people to charge their EVs since it can be done by simply plugging the EV to the outlet that is installed or nearby the parked car, thanks to integrated OBC, which is a serial of power converters [7].

The OBC has at the input an EMI filter in order to protect the system against electromagnetic interference. Then the front-end rectifier which transform the grid AC power to a continuous power to feed the battery. The second stage DC-DC converter has two principal reasons, the first is to provide a controlled wide range of DC power to charge the vehicle-mounted batteries, and the second one is the high frequency isolation between the AC input and the battery which is a critical requirement in On-Board chargers. Although the increase of switching frequency greatly reduces the volume of the transformer inductors, but it also brings about problems such as increasing switching loss, which decrease the efficiency, and increase electromagnetic interference. In order to solve these problems, soft switching technologies such as ZVS, ZCS, and LLC have emerged.

This paper is organized as follows: section II presents the front-end rectifier topologies. In section III, modelling and control design in charging mode is considered. After the design of the control theorical, a simulation results are presented, following the results discussion in section IV. Conclusion of the work is addressed in section V.

II. FRONT-END RECTIFIER TOPOLOGIES.

Boost **power** factor correction with bridge diode fig.2 is the simplest topology, and the most used in on board chargers. The working principle of this topology is that by controlling the switch we can magnetize and demagnetize the boost inductor, and then shape the current to follow the voltage waveform as a reference.
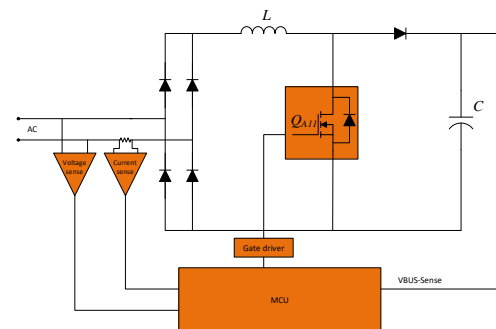

Fig.2 Boost PFC.

When the switch QA11 is Off the inductor magnetize and the current start increasing and when it's ON the inductor demagnetize and charge the capacitor then the current decreasing, the current waveform looks sinusoidal fig.3.
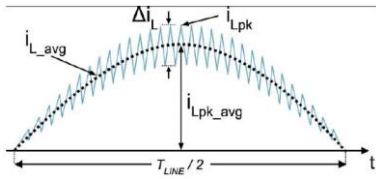

Fig.3 Current waveform with PFC.

It has a good result in the power factor, but there are drawbacks such as the two diodes in the main current path, which reduce the efficiency and increase heat, high total harmonic distortion. Furthermore, it's works in single phase only and when we implement the same topology in 3phas the power factor decreases.

fig.4 presents the totem-pole PFC topology. It is a conventional boost PFC where one half of the diode bridge is replaced by active switches S1 and S2 in a half bridge configuration, hence the name "totem pole" [1].
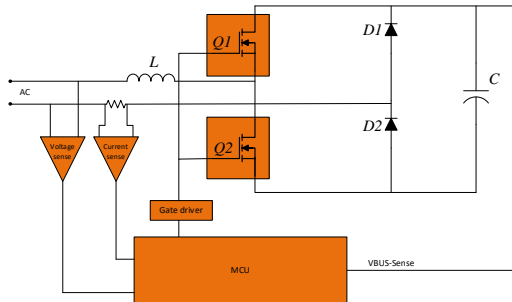

Fig.4 Totem pole topology.

In the positive AC line half-cycle, D2 is conducting and connecting the AC source to the output ground. Then the switch Q2 is the active boost switch and Q1 freewheels the inductor current and discharges inductor energy to power the output. In the negative AC line half cycle, D1 is conducting and connecting the AC source to the output DC bus. Q1 is the active boost switch and Q2 freewheels the inductor current. By these two cycles we can chape the current waveform and control it to have a sinusoidal and ohmic behavior of the AC input.

This topology reduces the amount of diode in the current path, but it is also a single-phase topology which limit the power level. The next section a technic of phase modular presented to use the totem pole topology and the boost PFC in the 3phase AC power in order to increase the power of the converter.

The phase-modular systems fig.5 use a single-phase rectifier stage for each phase, totem pole or full bridge boost PFC. Which means three rectifiers in one rectifier and the individual rectifier systems can either be connected in star or delta. The major advantage of this topology is the isolation between phases, so the system can work with phase losses.
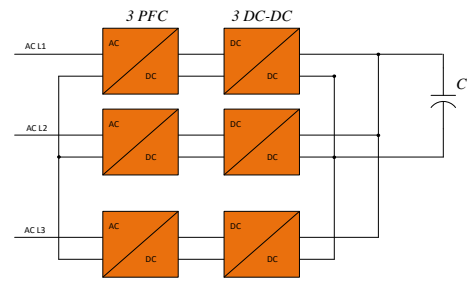

Fig.5 Phase modular topology.

As showed above, a DC-DC converter is required for each phase, so even if it shows good results these systems are not the first choice to achieve highest power density.

The six-switch PWM rectifier or Three-phase Two-level PFC fig.6 features a very simple circuit topology and easy control. It facilitates bidirectional power flow and can achieve a high power-factor with reasonable efficiency.
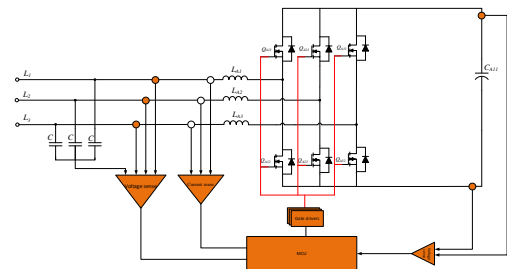

Fig.6 Three-phase Two-level PFC

Since this topology is a two-level topology, it requires high voltage blocking switches to block the entire DC link voltage. For example, in an 800-V DC link voltage application, a 1200-V rated blocking capacity Silicon Carbide (SiC) is required for the power stage, and switching losses are voltage dependent so if the voltage is increased power dissipation goes up as well, and it affects the long-term reliability of the semiconductor and other passive devices used in the power stage, which is one of the drawbacks of this topology. Another drawback is the bulky filter inductor which it requires to regulate the input current THD to low values. Hence, the power density is low compared to the other competitive multilevel PFC topologies which are documented such as "Vienna rectifier". [2]

The Vienna rectifier fig.7 developed in 1993 at the Technical University of Vienna, to avoid the occurrence of low-frequency mains current harmonics for unidirectional rectification, only by insertion of a turn-off semiconductor into each phase leg of a three-phase diode bridge [7,8].
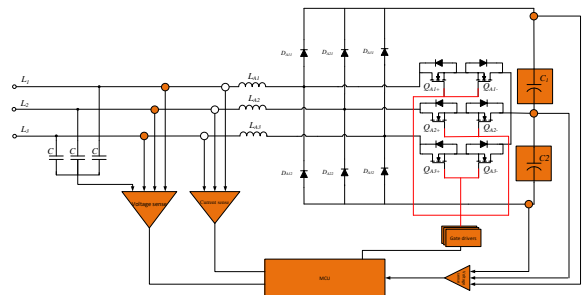

Fig.7 Vienna Rectifier.

The Vienna rectifier power topology is used in high-power, three-phase power factor correction applications. And it is popular due to its operation in continuous conduction mode (CCM), inherent multilevel switching (three level), also the selection of the blocking voltage capability of the power switches (FET field effect transistor), because it has to block only half of the output DC voltage and not the total output DC. For example, in an 800-V DC link voltage application, only a 600-V rated blocking capacity Si MOSFET is required for the power stage, and it reduce the power losses and ultimately reduce the cooling requirement, which increase the power density, for high power. Furthermore, it requires approximately only half of the inductance for the boost inductors compared to the two-level rectifiers discussed in Section 3.5. The multilevel signature of output voltage also provides a better THD performance. [3]

The only drawback of this topology is that it only supports unidirectional mode power transfer from the grid to the DC side and the control complexity of the midpoint voltage.

3phase T-Type converters presented in Fig.8 is an improvement of the Vienna topology in order to have a bidirectional power flow, and also an improvement of the two level PWM rectifier by having three level in order to reduce harmonics when it is in inverter mode. For 800-V DC link voltages, the high-side and the low-side on each phase would usually be implemented with 1200-V IGBTs/MOSFET as the full voltage has to be blocked. Differently, the bidirectional switch to the DC-link midpoint has to block only half of the DC link voltage. It can be implemented with devices having a lower voltage rating like two 600-V IGBTs including antiparallel diodes. Due to the reduced blocking voltage, the middle switch shows very low switching losses and acceptable conduction loss.
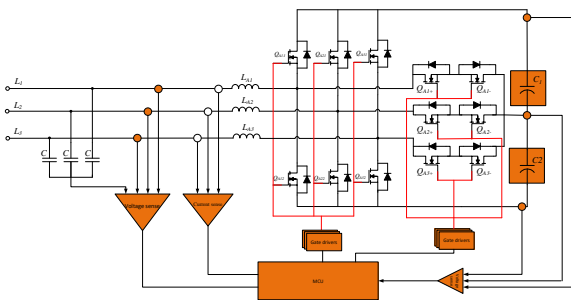

Fig.8 Triphase 3level T-type PFC (Bidirectional Vienna topology).

In order to have a high-power On-Board charger with high power density, a single-phase topology is not a good option, therefore, the selected is a three-phase topology, and based on the classification above if a bidirectional power flow is not necessary the Vienna rectifier provides excellent performance in terms of the efficiency, power factor and power density.

So, in the first step we choose Vienna rectifier topology for Grid to vehicle power direction, and an extension of power direction from Vehicle to the grid V2G or Vehicle to Vehicle V2V by the 3level T-type topology.
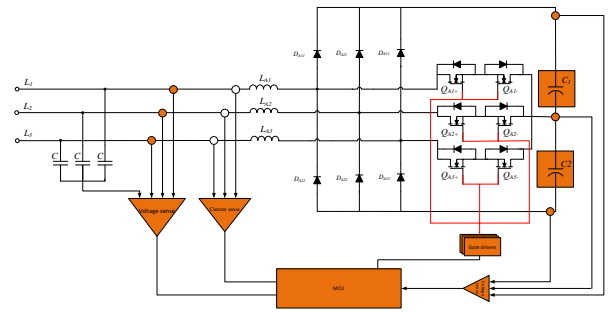

Fig.9 shosen topology.

III. MODELING AND CONTROL DESIGN IN CHARGING MODE

In the past several years, there has been a lot of research done on this aspect, where only some include the DC Bus equalization, in order to balance the voltage across the positive and negative capacitor C1 and C2.

These researches present many control methods for the Vienna rectifier, starting by the simplest control method, which is the hysteresis control, but it's not recommended since the switching frequency is variable which makes defining power losses harder. Another control method largely used for this topology is the space vector modulation SVM [8,9].

And there are a few researchers that investigated in the d-q average model and PI control of the Vienna rectifier, which we'll go through in our modeling based on a thesis made by the microchip company in collaboration with North Carolina State University. The three active switching units Qa, Qb, and Qc are controlled to ensure sinusoidal ac current and steady dc-link voltage. Since this type of rectifier is current force commutated, the rectifier pole voltage (VAN, VBN, VCN) is determined by not only the controlled switch state but also the polarity of the ac phase current at the corresponding instance.
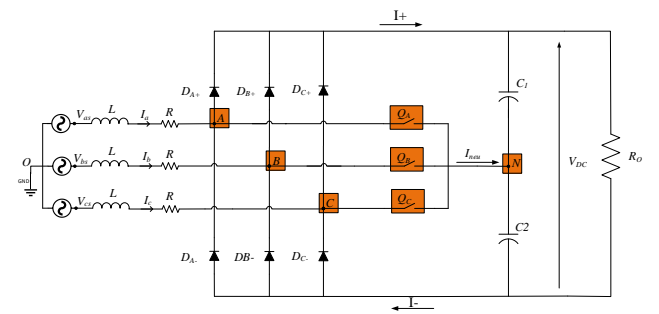

Fig.10 Simplified Vienna rectifier.

The current state space presentation can be:

$$\begin{cases} L\dfrac{di_a}{dt} = V_{as} - Ri_a - V_{AN} - V_{NO} \\ L\dfrac{di_b}{dt} = V_{bs} - Ri_b - V_{BN} - V_{NO} \\ L\dfrac{di_c}{dt} = V_{cs} - Ri_C - V_{CN} - V_{NO} \end{cases} \quad (1)$$

Where VNO is the voltage across the neutral point of the dc-link and the neutral point of the three-phase input voltage, and L is the input inductance. V_{as}, V_{bs}, and V_{cs} are the input source voltages.

If we do the SUM of the three equations then the V_{NO} can be:

$$3V_{NO} = (V_{as} + V_{bs} + V_{cs}) - L\frac{d(i_a + i_b + i_c)}{dt} - R(i_a + i_b + i_c) - (V_{AN} + V_{BN} + V_{CN})$$

If we suppose that the AC source as a balanced source:

$$\begin{cases} L\dfrac{d(i_a + i_b + i_c)}{dt} = 0 \\ R(i_a + i_b + i_c) = 0 \\ (V_{as} + V_{bs} + V_{cs}) = 0 \end{cases} \qquad (3)$$

Then:

$$V_{NO} = \frac{1}{3}(V_{AN} + V_{BN} + V_{CN}) \qquad (4)$$

- If the switch Q_a is off and the phase current ia is positive, the phase leg A is clamped to the positive dc link, and therefore, V_{AN} is equal to $\frac{V_{DC}}{2}$.
- Similarly, if Q_a is off and iA is negative, then VAN will be $-\frac{V_{DC}}{2}$.
- If the Q_a is on, phase leg A will be clamped to the dc-link neutral point and VAN will be zero, regardless of ia polarity.

The same operation principle applies to phase B and phase C. Based on this understanding, state-space representation can be obtained, and then used to analyze the system operation. So, if we suppose that:

$$Sx = \begin{cases} 0 & Q_x \ is \ OFF \\ 1 & Q_x \ is \ ON \end{cases} \qquad (5)$$

$$sng(i_x) = \begin{cases} 1 & i_x \geq 0 \\ -1 & i_x \leq 0 \end{cases} \qquad (6)$$

Then the voltage across V_{XN} can be:

$$\begin{cases} V_{AN} = \dfrac{Vdc}{2}sng(i_a)(1 - Sa) \\ V_{BN} = \dfrac{Vdc}{2}sng(i_b)(1 - Sb) \\ V_{CN} = \dfrac{Vdc}{2}sng(i_c)(1 - Sc) \end{cases} \qquad (7)$$

And the duty cycle dx is defined as:

$$d_{a,b,c} = sng(i_{a,b,c})\left(1 - \frac{T_{a,b,c}}{T_s}\right)$$
$$= sng(i_{a,b,c})((1 - K_{a,b,c}) \qquad (8)$$

$\frac{T_{a,b,c}}{T_s}$ represents the average switch on-time for Qa, Qb, and Qc in one switching cycle, respectively. Then, the V_{XN} can be:

$$\begin{cases} V_{AN} = \dfrac{Vdc}{2}d_{a,} \\ V_{BN} = \dfrac{Vdc}{2}d_b \\ V_{CN} = \dfrac{Vdc}{2}d_b \end{cases} \qquad (9)$$

Based on this understanding, state-space representation can be obtained, and then used to analyze the system operation.

$$\begin{cases} L\dfrac{di_a}{dt} = V_{as} - Ri_a - (\dfrac{Vdc}{2}da - \dfrac{Vdc}{6}(d_a + d_b + d_c)) \\ L\dfrac{di_b}{dt} = V_{bs} - Rib - (\dfrac{Vdc}{2}db - \dfrac{Vdc}{6}(d_a + d_b + d_c)) \\ L\dfrac{di_c}{dt} = V_{cs} - Ric - (\dfrac{Vdc}{2}dc - \dfrac{Vdc}{6}(d_a + d_b + d_c)) \end{cases} \qquad (10)$$

If we put $d'_{a,b,c} = d_{a,b,c} - d_0$ where $d_0 = \frac{1}{3}(d_a + d_b + d_c)$. $d'_{a,b,c}$ and d_0 are the sinusoidal components and the zero-sequence component, respectively. Then the Model in the ABC reference become eq.11:

$$\begin{cases} L\dfrac{di_a}{dt} = V_{as} - Ri_a - \dfrac{Vdc}{2}d'_a \\ L\dfrac{di_b}{dt} = V_{bs} - Rib - \dfrac{Vdc}{2}d'_b \\ L\dfrac{di_c}{dt} = V_{cs} - Ric - \dfrac{Vdc}{2}d'_c \end{cases} \qquad (11)$$

The Laplace transform of the model is:

$$L\frac{di_x}{dt} + Ri_x = V_x - \frac{Vd_c}{2}d'_x$$
$$\Rightarrow \quad (L_s + R)i_x = V_x - \frac{Vd_c}{2}d'_x \qquad (12)$$

Then the basic structure of **the current model** of the Vienna rectifier can be illustrated as:
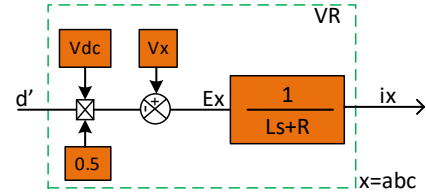

Fig.11 current model of the Vienna rectifier.

The same for the output voltage, which depends on the amount of current delivered by the input, and the different voltage across the two capacitor is also depend on the state of the switches. And based on the fig.9 the state space model can be:

$$\begin{cases} C_0\dfrac{dv_{C1}}{dt} = i^+ - \dfrac{V_{dc}}{R_0} \\ C_0\dfrac{dv_{C2}}{dt} = i^- - \dfrac{V_{dc}}{R_0} \end{cases} \qquad (13)$$

The voltage across the two capacitors will be:

$$C_0\frac{dV_{dc}}{dt} = i^+ + i^- - 2\frac{V_{dc}}{R_0} \qquad (14)$$

where i+ and i− are the currents through the positive and negative capacitor of the dc bus, respectively. According to Kirchhoff's current law, i+ and i− are given as:

$$\begin{cases} i^+ = i_{DA^+} + i_{DB^+} + i_{DC^+} \\ i^- = i_{DA^-} + i_{DB^-} + i_{DC^-} \end{cases} \qquad (15)$$

where iD(A,B,C)+ and iD(A,B,C)− are the currents passed through the top and bottom diodes for difference phases. The current through the top diode is depend on the current sign and the switch state, therefore the equation of this current is:

$$i_{D(A,B,C)^+} = \begin{cases} (1 - K_{a,b,c})i_{A,B,C} \ (i_{A,B,C} \geq 0) \\ 0 \qquad (i_{A,B,C} < 0) \end{cases} \qquad (16)$$

The same for the bottom diode the current is null when the midpoint switch is OFF, or the current sign is positive.

$$i_{D(A,B,C)^-} = \begin{cases} 0 & (i_{A,B,C} \geq 0) \\ -(1 - K_{a,b,c})\, i_{A,B,C} & (i_{A,B,C} < 0) \end{cases} \qquad (17)$$

By subtracting and summing these two equations the result is:

$$i_{D(A,B,C)^-} - i_{D(A,B,C)^+} = -(1 - K_{a,b,c})\, i_{A,B,C} \qquad (18)$$

$$i_{D(A,B,C)^+} + i_{D(A,B,C)^-} = sng(i_{a,b,c})(1 - K_{a,b,c}) \qquad (19)$$
$$= d_{a,b,c} i_{A,B,C}$$
$$\Rightarrow \quad i^+ + i^- = d_a i_A + d_b i_B + d_c i_C \qquad (20)$$

By subtracting the the zero-sequence component d0 $(i_A + i_B + i_C) = 0$ the equation become with d'.

$$i^+ + i^- = d_a i_A + d_b i_B + d_c i_C - d_0(i_A + i_B + i_C)$$
$$\Rightarrow \quad i^+ + i^- = d'_a i_A + d'_b i_B + d'_c i_C \qquad (21)$$

From (14) and (21) the output stage model become:

$$C_0 \frac{dV_{dc}}{dt} = d'_a i_a + d'_b i_b + d'_c i_c - 2\frac{V_{dc}}{R_0} \qquad (22)$$

Based on the input and the output stage model (11) and (22), the Vienna rectifier averaged model can be derived from this:

$$\begin{cases} L\frac{di_a}{dt} = V_{as} - Ri_a - \frac{Vdc}{2}d'_a \\ L\frac{di_b}{dt} = V_{bs} - Rib - \frac{Vdc}{2}d'_b \\ L\frac{di_c}{dt} = V_{cs} - Ric - \frac{Vdc}{2}d'_c \\ C_0\frac{dV_{dc}}{dt} = d'_a i_a + d'_b i_b + d'_c i_c - 2\frac{V_{dc}}{R_0} \end{cases} \qquad (23)$$

With park transformation and the model equation in the ABC reference (23), we can find the input current model in the synchronous dq reference by this equation.

$$\begin{cases} V_{sd} = L\frac{di_d}{d_t} - \omega_0 L i_q + Ri_d + \frac{V_{dc}}{2}d'_d \\ V_{sq} = L\frac{di_q}{d_t} + \omega_0 L i_d + Ri_q + \frac{V_{dc}}{2}d'_q \end{cases} \qquad (24)$$

And the Laplace transform:

$$\begin{cases} Lsi_d + Ri_d = V_{sd} - \omega_0 L i_q - \frac{V_{dc}}{2}d'_d \\ Lsi_q + Ri_q = V_{sd} - \omega_0 L i_d - \frac{V_{dc}}{2}d'_q \end{cases} \qquad (25)$$

then by the decoupling method we can create new variables as:

$$\begin{cases} E_d = V_{sd} - \omega_0 L i_q - \frac{V_{dc}}{2}d'_d \\ E_q = V_{sq} - \omega_0 L i_d - \frac{V_{dc}}{2}d'_q \end{cases} \qquad (26)$$

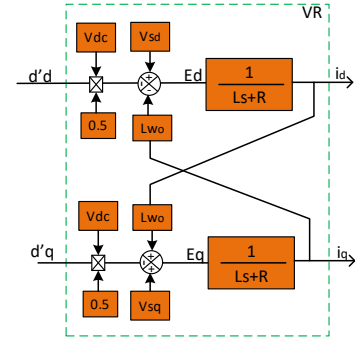Which can be illustrated as:

Fig.12 Current model illustration in the DQ reference.

Same approach for the DC stage with the Park transformation and the equation (23), the model in the dq reference will be:

$$C_0 \frac{dV_{dc}}{dt} = d'_d i_d + d'_q i_q - 2\frac{V_{dc}}{R_0} \qquad (27)$$

From the equations (27) and (25) the Vienna rectifier's model in this reference will be:

$$\begin{cases} V_{sd} = L\frac{di_d}{d_t} - \omega_0 L i_q + Ri_d + \frac{V_{dc}}{2}d'_d \\ V_{sq} = L\frac{di_q}{d_t} + \omega_0 L i_d + Ri_q + \frac{V_{dc}}{2}d'_q \\ C_0\frac{dV_{dc}}{dt} = d'_d i_d + d'_q i_q - 2\frac{V_{dc}}{R_0} \end{cases} \qquad (28)$$

Since we've the model in the both reference, control design is no longer a big issue. So based on the model we designed the control, and with the dq reference we can have the advantage of the PI or PID controller.

As shown in fig.12 The control has an inner and outer loop, the outer loop is the voltage control, which define the amount current need to be feed to the output capacitor in order to achieve the desired voltage, and this current define the reference of the input current which define the duty cycle that should the bidirectional switch keep conducting.

The output of the current loop controllers is passes through an inverse Park transformation and is modulated using sinusoidal modulation (not space vector modulation).
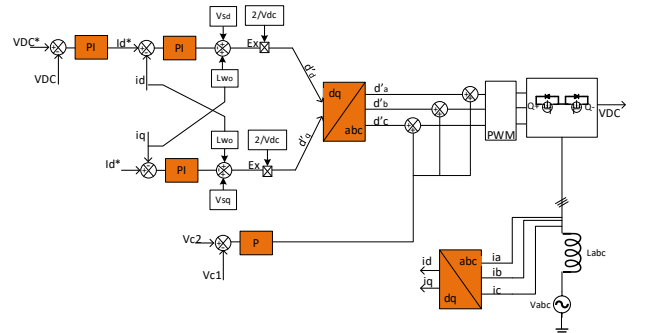

Fig.13 The control architecture

IV. RESULTS AND DISCUSSION

After the design of the control theorical, and many simulations test we get a few errors during the simulation, therefore, PI parameters are adjusted empirically in order

to improve the simulation result. In this simulation the main point to supervise are:

- Power factor correction
- Input current waveform, which has to be sinusoidal.
- Output voltage stability around 800VDC.
- DC Bus equalization, balancing the voltage across the positive and negative capacitor at 400VDC for each.

Ohmic fundamental mains behavior or unity power factor is the goal behind PFC, based on the literature the Vienna rectifier can achieve PFC close to 0.997 [4], in our simulation in the steady state the power factor is 0.9961.

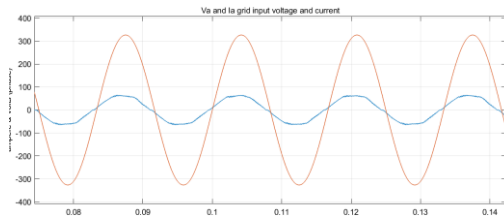Also, the fig.14 shows that the grid current has a sinusoidal waveform, and in phase with input voltage.

Fig.14 PFC Results.

During the charging time of the capacitor "Precharge" the power factor was 94% because the precharge circuit limit the current even with boost PFC but after the precharge delay and the precharge relay is conducting the control get the power factor the interval [0.99:1].

In order to check the stability of the output voltage for different loads, the controlled current source is a great choice for varying the load. In this simulation a 30kw load as a principal load and two other of 4kw programmed, first one for 0.15ms for the entire DC voltage 800V and the second one is for 0.23ms and it is connected to the VC2=400V side only.
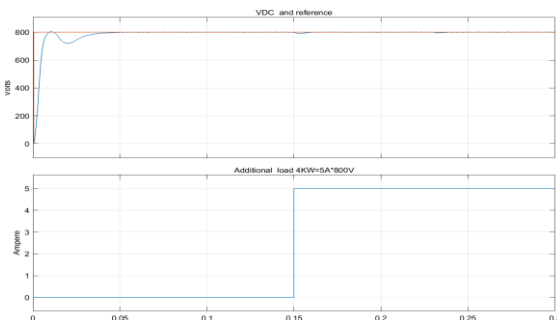

Fig.15 The output voltage scope.

The output of the rectifier is connected to two dual active bridge DC-DC. Therefore, balancing the voltage across the two capacitor is necessary, and each capacitor voltage should be equal to half the output voltage at the steady state.
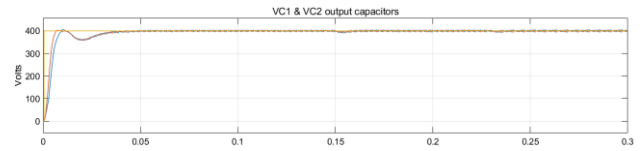

Fig.16 DC Bus equalization.

Testing the controller for unbalanced input voltage and an over voltage is a must, in order to validate the control scheme. The result of a 440VAC is a 10% overshot on the output Voltage which is not a bad result, the PFC and other performance are still good. By adding a resistor in one phase only, the three phases grid become unbalanced the dynamic response of the system become slower.

V.   CONCLUSION

This paper proposed a bidirectional On-Board charger with an efficient topology, which reduced the component stress and increased the power factor. And it derived a control method in the charging G2V mode, the next step is the control design in V2G mode and the hardware design for experimental evaluation and analysis.

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